DO Upgrade Schedule
Fiber Electronics

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WB$	Resource Names
914	FIBER TRIGGER ELECTRONICS FABRICATION	318.2 w	10/3/94	2/12/01		As Soon As		
915	SVX II	192.6 w	10/1/96	8/25/00		As Soon As		
916	*SVXII Rad Hard Chips Available*	*0 w*	*10/1/96*	*10/1/96*		*Start No Ear*		
917	SVX II+Pick Off Packaging Proto.	54 w	10/1/96	10/30/97	916	As Soon As F		EEF115[0.2],EEU115[0.5]
918	Pickoff chip-third prototype	19 w	11/5/97	4/1/98		Start No Earl		EEF115[0.5],PhysF115[0.5]
919	*M3-Fiber Trigger Pickoff Chips Ordered*	*0 w*	*7/1/97*	*7/1/97*		*As Soon As*		
920	Pickoff Chip Production	16 w	11/19/98	3/26/99	918FS+6 w,919	Start No Earl	1.1.5.3.1.2(.28)	PhysU115,PhysF115[0.3],EEF115[0.5],k$[0.15],k$c[0.03]
921	*Multichip Modules Ordered*	*0 w*	*10/20/97*	*10/20/97*		*Start No Ear*		
922	Multichip Module Preproduction	77 w	11/26/97	6/24/99	920FF+4 w,921FS+4 w	Finish No Ea	1.1.5.3.1.1,1.1.5.3.1.2(.72),1.1.5	EEF115[0.5],k$[8.48],k$c[0.65]
923	Final Production - MCM	32 w	1/13/00	8/25/00	935	As Soon As F		ETF115,EEF115
924	*Multichip Modules Received*	*0 w*	*8/25/00*	*8/25/00*	*923*	*As Soon As*		
925	FE Analog Boards	318.2 w	10/3/94	2/12/01		As Soon As		
926	Analog Board Prototype	34 w	11/1/95	7/2/96		Start No Earl		EEF115[0.5],ETF115[0.5],PhysF115[0.3]
927	Procure Parts - FY95	16 w	10/3/94	1/20/95	926	Start No Earl	1.1.5.3.2.2,1.1.5.3.2.3	k$[0.2],k$c[0.04]
928	Procure Parts - FY96	16 w	10/2/95	1/25/96	927	Start No Earl	1.1.5.3.1.8,1.1.5.3.1.11(.5),1.1.5	k$[2.18],k$c[0.09]
929	Analog Board Test with Cassette	35 w	4/13/98	12/23/98	928	As Soon As F		PhysU115,PhysF115[0.3]
930	*M3-Fiber Tracker Analog Board Test Complete*	*0 w*	*12/23/98*	*12/23/98*	*929*	*As Soon As*		
931	Preproduction Boards	70.8 w	4/1/99	8/31/00		As Soon As		
932	8-chip boards	32 w	4/1/99	11/15/99		Start No Earl		
933	12-chip boards	44.8 w	10/5/99	8/31/00	932FS-6 w	As Soon As F		
934	Final Test	44.8 w	11/16/99	10/13/00		As Soon As		
935	8-chip test	6 w	11/16/99	1/12/00	922,932	As Soon As F		PhysU115[2],PhysF115[0.6],ETF115[0.5]
936	12-chip test	6 w	9/1/00	10/13/00	933	As Soon As F		PhysU115[2],PhysF115[0.6],ETF115[0.5]
937	Redesign and Test Boards	42.8 w	1/13/00	11/10/00		As Soon As		
938	8-chip board	20.4 w	1/13/00	6/5/00	935	As Soon As F		PhysU115[2],PhysF115[0.6],ETF115[0.5]
939	12-chip board	4 w	10/16/00	11/10/00	936	As Soon As F		PhysU115[2],PhysF115[0.6],ETF115[0.5]
940	Bid Production	46.8 w	11/16/99	10/27/00		As Soon As		
941	Bid 8-chip board production	8 w	11/16/99	1/26/00	932	As Soon As F		
942	Bid 12-chip board production	8 w	9/1/00	10/27/00	933	As Soon As F		
943	8-chip Board Production	40.4 w	1/26/00	11/8/00		As Soon As		
944	*M3-Fiber Tracker 8-chip Analog Boards Ordered*	*0 w*	*1/26/00*	*1/26/00*	*941,935*	*As Soon As*	*1.1.5.3.3.4,1.1.5.3.3.5(.78),1.1.5*	*k$[1.06],k$c[0.19]*
945	Produce 10 8-chip boards	4 w	6/6/00	7/3/00	923SS+6 w,944,938	As Soon As F		EEF115[2],ETF115[1.5]
946	*Ten 8-chip Analog Boards Available*	*0 w*	*7/3/00*	*7/3/00*	*945*	*As Soon As*		
947	Test 10 8-Chip Boards	6 w	7/5/00	8/15/00	946	As Soon As F		EEF115,ETF115
948	Produce and test remaining 8-chip boards	12 w	8/16/00	11/8/00	947	As Soon As F		EEF115[2],ETF115[1.5]
949	*8-chip Analog Boards Ready*	*0 w*	*11/8/00*	*11/8/00*	*948*	*As Soon As*		
950	12-chip Board Production	14 w	10/27/00	2/12/01		As Soon As		
951	*M3-Fiber Tracker 12-chip Analog Boards Ordered*	*0 w*	*10/27/00*	*10/27/00*	*942,936*	*As Soon As*		
952	Produce 10 12-chip boards	4 w	11/13/00	12/12/00	951,939,923SS+6 w	As Soon As F		
953	*Ten 12-chip Analog Boards Available*	*0 w*	*12/12/00*	*12/12/00*	*952*	*As Soon As*		
954	Test ten 12-Chip Boards	2 w	12/13/00	12/28/00	953	As Soon As F		
955	Produce and test remaining 12-chip boards	6 w	1/2/01	2/12/01	954	As Soon As F		
956	*12-chip Analog Boards Ready*	*0 w*	*2/12/01*	*2/12/01*	*955*	*As Soon As*		
957	CFT Digital Boards	192.25 w	11/12/96	10/6/00		As Soon As		
958	Development	81 w	11/12/96	7/7/98		Start No Earl		EEU115
959	Test Board Prototype Fabrication	4 w	1/4/99	1/29/99		Start No Earl		EEF115[0.3],ETF115[0.5]
960	*Test Board Prototype Complete*	*0 w*	*1/29/99*	*1/29/99*	*959*	*As Soon As*		
961	Board Test	12 w	2/1/99	4/23/99	917,959	As Soon As F		PhysU115,PhysF115[0.3],EEF115,ETF115[0.5]
962	Final Design	28 w	4/1/99	10/18/99		As Soon As		
963	Design Motherboard	6 w	4/1/99	5/12/99		Start No Earl		EEF115,ETF115[0.5]
964	Design Level 1 Daughter Board	20 w	5/13/99	10/4/99	963	As Soon As F		EEF115,ETF115[0.5],PhysF115
965	Design Level 2 Daughter Board	22 w	5/13/99	10/18/99	963	As Soon As F		EEF115[2],ETF115[0.5]
966	Final Prototypes	35 w	5/13/99	2/2/00		As Soon As		
967	Mother Board Prototype	6 w	5/13/99	6/24/99	963	As Soon As F		EEF115,ETF115[0.5]
968	Level 1 Daughter Board Prototype	10 w	10/5/99	12/15/99	964	As Soon As F		EEF115,ETF115[0.5]
969	Level 2 Daughter Board Prototype	13 w	10/19/99	2/2/00	965	As Soon As F		EEF115,ETF115[0.5]
970	Final Test	25 w	12/16/99	6/22/00		As Soon As		
971	Test Mother Board and Level 1 Daughter Board	6 w	12/16/99	2/9/00	967,968	As Soon As F		PhysU115,PhysF115[0.3],EEF115,ETF115[0.5]
972	Test Mother Board and Level 2 Daughter Board	20 w	2/3/00	6/22/00	967,969	As Soon As F		PhysU115,PhysF115[0.3],EEF115,ETF115[0.5]
973	Redesign	21 w	2/10/00	7/7/00		As Soon As		
974	Motherboard Redesign	4 w	2/10/00	3/8/00	971	As Soon As F		PhysU115[0.5],PhysF115[0.1],EEF115[0.5],ETF115[0.25]
975	Level 1 Daughter Board Redesign	3 w	2/10/00	3/1/00	971	As Soon As F		PhysU115[0.5],PhysF115[0.1],EEF115[0.5],ETF115[0.25]
976	Level 2 Daughter Board Redesign	2 w	6/23/00	7/7/00	972	As Soon As F		PhysU115[0.5],PhysF115[0.1],EEF115[0.5],ETF115[0.25]
977	Bid Mother and Daughter Boards	12.6 w	10/19/99	1/31/00	962	As Soon As F		
978	*M3-CFT Digital Boards Ordered*	*0 w*	*1/31/00*	*1/31/00*	*977*	*As Soon As*		
979	Produce 10 Boards	8 w	5/16/00	7/13/00	973SS+65 %,978	As Soon As F	1.1.5.3.1.3,1.1.5.3.1.5-1.1.5.3.1.	EEF115,ETF115[0.5],k$[1.98],k$c[0.38]
980	*10 Digital Boards Available*	*0 w*	*7/13/00*	*7/13/00*	*979*	*As Soon As*		
981	Test Boards	4 w	7/13/00	8/10/00	980	As Soon As F		
982	Final Production	8 w	8/10/00	10/6/00	981	As Soon As F	1.1.5.3.6.3,1.1.5.3.6.5-1.1.5.3.6.	EEF115,ETF115[0.5],k$[2.7],k$c[0.49]
983	*CFT Digital Boards Ready*	*0 w*	*10/6/00*	*10/6/00*	*982*	*As Soon As*		
984	Mixer Boards	80.8 w	4/1/99	11/10/00		As Soon As		
985	Test Board Design	19 w	4/1/99	8/13/99		Start No Earl		EEF115[0.5]

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WB$	Resource Names
986	Test Board Prototype	9.8 w	8/16/99	10/22/99	985	As Soon As I		EEF115
987	Prepare Final Design	26 w	12/1/99	6/14/00	986	Start No Earl		EEF115
988	*Mixer Board Design Finished*	*0 w*	*6/14/00*	*6/14/00*	*987*	*As Soon As*		
989	Build Mixer Prototype	11 w	6/15/00	8/31/00	988	As Soon As I		EEF115,ETF115[0.2]
990	Redesign Mixer Board	2 w	9/1/00	9/15/00	989	As Soon As I		EEF115
991	Bid Mixer Boards	6 w	6/15/00	7/27/00	986,987	Start No Earl		
992	*Mixer Boards Ordered*	*0 w*	*9/15/00*	*9/15/00*	*990,991*	*As Soon As*	*1.1.5.3.8*	*k$[1.27],k$c[0.26]*
993	Build Production Boards	8 w	9/18/00	11/10/00	990,992	As Soon As I		EEF115[0.5]
994	*Mixer Boards Ready*	*0 w*	*11/10/00*	*11/10/00*	*993*	*As Soon As*		
995	**Support Hardware**	**69.4 w**	**5/17/99**	**10/6/00**		**As Soon As**		
996	Design FEA Backplane	4 w	5/17/99	6/14/99		Start No Earl		EEF115
997	Produce FEA Backplane	11 w	10/11/99	1/11/00		As Soon As I	1.1.5.3.1.11(.5),1.1.5.3.3.10(.5)	k$[0.09],k$c[0.02]
998	Design Motherboard Backplanes	4 w	9/1/99	9/29/99	962	As Soon As I		EEF115
999	Produce Motherboard Backplanes	15 w	9/30/99	1/28/00	998	As Soon As I	1.1.5.3.6.11(.67),1.1.5.3.7.10	k$[0.11],k$c[0.02]
1000	Design Mixer Board Backplanes	4 w	6/15/00	7/13/00	987	As Soon As I		EEF115
1001	Produce Mixer Board Backplanes	12 w	7/14/00	10/6/00	1000	As Soon As I		
1002	Rack Prep in Movable Counting House	30 w	5/1/97	12/3/97		Start No Earl		EEF115[0.2],ETF115
1003	Install cable ways and fiber tracker electrical cables	10 w	5/8/00	7/18/00	524SS-4 w	As Soon As I		MTF115[2],Platform
1004	Installation & System Test	12 w	11/13/00	2/12/01	948,982SS+50 %,993,955FF	As Soon As I		EEF115[3],PhysU115[2],PhysF115,ETF115,Platform[0.7],MCH1
1005	*First Crate Operational*	*0 w*	*8/15/00*	*8/15/00*	*947*	*As Soon As*		